

ABSTRACT

A plurality of memory devices can be erase block tagged in parallel by issuing an erase pulse to memory devices that do not have memory blocks with erase block latches that indicate the block is erased. The status of the memory block is read after the erase pulse. If there are blocks remaining to be erased, erase block tag patterns are generated. Each memory block at a particular sector address has a unique erase block tag pattern to set the erase block latch for that particular memory block. The patterns are transmitted in parallel to the memory devices in a data burst.